

## RESEARCH ARTICLE

# Simulation and Comparison of Voltage and Current Characteristics of Novel Finfet by Varying its Oxide Thickness with Single Gate Mosfet for Improved Conductivity

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### ABSTRACT

**Aim:** The current and voltage characteristics of FinFET and single gate MOSFET are simulated by varying their oxide thickness ranging from 2 nm to 20 nm. **Materials and Methods:** The electrical conductance of FINFET (n= 320) was compared with MOSFET (n=320) by varying oxide thickness ranging from 2 nm to 20 nm in the NANO HUB tool simulation environment. **Results:** FINFET has significantly higher conductance ( $2.66 \times 10^{-4}$  mho  $P < 0.05$ ) than single gate MOSFET ( $1.64 \times 10^{-4}$  mho). The optimal thickness for maximum conductivity was 2nm for FINFET, and 2 nm for MOSFET. **Conclusion:** Within the limits of this study, FINFET with oxide thickness of 2 nm offers the best conductivity.

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### Introduction

Current and voltage characteristics of FinFET and single gate MOSFET are being explored through simulation by varying the oxide thickness of the device. Reducing the size of Bulk CMOS technology has become extremely difficult due to large short channel effects (Frank et al. 1992). FinFET have been viewed as the adaptable CMOS technology because of their resistance towards the short channel effect (SCE), better current drive and practically ideal subthreshold slope [(Taur 2001)]. M. Masahara and D. Fried explained that the IV characteristics of FinFET can be used to determine the current and voltage characteristics of the triple gate FinFET structure in the future and it can also be used for the fabrication of highly efficient FinFET which can be used as an amplifier as well as a switch. (Masahara et al. 2005), (Fried et al., n.d.).

Several research articles were published on FinFET in the past 5 years. 95 research articles were published in IEEE explore and 413 research articles were published in science direct. In recent times FinFETs were explored mostly as they were seen as the transistors with full potential for ultra-scaled CMOS integrated circuits (Huang et al., n.d.). Most of the research deals with the technical features of FinFET and short channel performance, there are hardly any studies that deals with the analysis of physical features and mobility of electrons in the channel (Yu et al., n.d.), (Rudenko et al. 2005), (Kavalieros et al., n.d.). Kavalieros et al explained about dielectric capacitance and mobility of carriers in the channel which are the important features of FinFETs. Even though there wasn't any proper recognition for dielectric capacitance of FinFETs, it can entirely influence several device variables. Split C-V measurements were used to analyse mobility and capacitance of narrow fin devices along with wide fin devices, which helps in understanding the

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behaviour of FinFETs better. (Lindert et al., n.d.), (Chaudhuri, Mishra, and Jha 2012), (Ren et al. 2002).

Previously our team has a rich experience in working on various research projects across multiple disciplines (Sathish and Karthick 2020; Varghese, Ramesh, and Veeraiyan 2019; S. R. Samuel, Acharya, and Rao 2020; Venu, Raju, and Subramani 2019; M. S. Samuel et al. 2019; Venu, Subramani, and Raju 2019; Mehta et al. 2019; Sharma et al. 2019; Malli Sureshbabu et al. 2019; Krishnaswamy et al. 2020; Muthukrishnan et al. 2020; Gheena and Ezhilarasan 2019; Vignesh et al. 2019; Ke et al. 2019; Vijayakumar Jain et al. 2019; Jose, Ajitha, and Subbaiyan 2020). Now the growing trend in this area motivated us to pursue this project.

Since shrinking of the devices are increasing, the issues with the planar or bulk Si-CMOS technology are also increasing. Several short channel impacts like increased leakage current, gate induced drain leakage (GIDL), sub threshold S/D spillage, gate direct tunnelling leakage, drain induced barrier lowering (DIBL), and hot carrier effects are degrading the usage of bulk Si-CMOS technology in the industry. These exclusive characteristics and current and voltage properties of FinFET inspired us to perform a few simulations based research with respect to FinFET by differing some of the parameters of this device. Oxide thickness of the device plays a significant role in the current and voltage properties of FinFET. The main aim of the study is to replace single gate MOSFET with FinFET because of its better performance for the same amount of energy provided (Mishra and Jha 2010), (Leonelli et al. 2011), (Meindl 1995), (Hu et al. 2000).

## Materials and Methods

In this research work there are two groups. One group refers to FinFET and the other group refers to single gate MOSFET. The pre-test analysis was done using *clinicalc.com* by keeping g-power at 80%, threshold at 0.05%, confidence interval at 95% (Patcharasardra and Pengchan 2016), (Saha et al. 2020). For each group the sample size is 320. The total sample size of the research work is 640.

In sample preparation for group 1, current and voltage characteristics of FinFET are analysed by varying oxide thickness ranging from 2nm to 20nm using the Nano Hub tool. In order to simulate FinFET first open Nano Hub in any one of the available search engines. Select resources in the NanoHub home page and select tools. Select FinFET in tags and select MugFET in the next box and then launch the tool. After launching the tool, go to the structure and change the oxide thickness of two fins. For each change in oxide thickness with an interval of 1nm select on simulate to get results for the respective values.

In sample preparation for group 2, current and voltage characteristics of single gate MOSFET were analysed by varying oxide thickness ranging from 2nm to 20nm using the NanoHub tool. In order to simulate the single gate MOSFET, first open Nano Hub in any one of the available search engines. Select resources in the NanoHub home page and select tools. Select MOSFET in tags and select on MOSFET in the next box and then launch the tool. After launching the

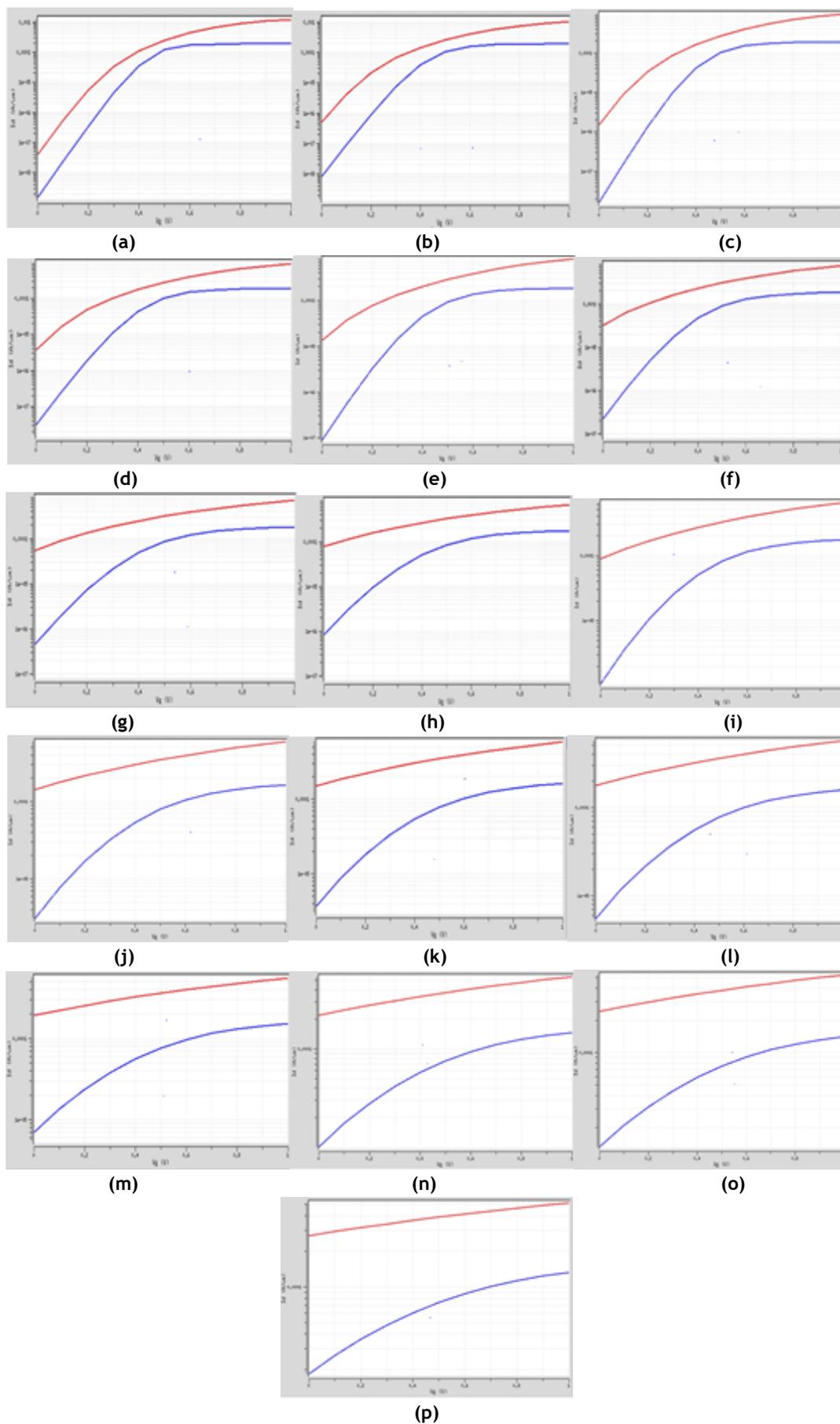
tool, go to structural properties and change the oxide thickness of single gate MOSFET. For every change in oxide thickness with an interval of 1nm and select on simulate to get results for the respective values.

Nano Hub is an open-source software tool. It is a science and engineering gateway comprising several resources that are useful for educational and research purposes. Nano Hub consists of predefined simulation tools for nanotechnology that are used to perform simulations instead of doing experiments physically. Since it is a software tool the results are precise and accurate. The testing procedure measures the current and voltage characteristics of FinFET and single gate MOSFET. Keep the gate voltage as constant (0.6v) and note down drain current. Similarly simulate for remaining values and note down drain current by keeping gate voltage as constant (0.6v) and tabulate them. Conductance of FinFET and single gate MOSFET is obtained by dividing the respective drain current with gate voltage (0.6v).

The statistical software used in this research work are origin and SPSS. Origin is used to plot graphs for given values and compare the variables and SPSS is used to calculate the mean, standard deviation and significance difference of the results obtained through simulation. In this research work oxide thickness and gate voltage are the independent variables since they are inputs and remain constant even after changing other parameters, whereas the drain current and conductance are dependent variables because they depend on the inputs and vary for every change in the input. The analysis of the research work is done using Independent T-Test, which is used to compare conductance and drain current of FinFET and single gate MOSFET. Oxide thickness is the independent variable and conductance and drain current are the dependent variables.

## Results

Current and voltage characteristics of FinFET and single gate MOSFET for oxide thickness (2nm-19nm) are shown in (Fig 1) and (Fig 3) respectively. For every change in the oxide thickness of the device, drain current is tabulated by keeping gate voltage as 0.6v as shown in (Table 1). (Fig 2) shows the graphical representation of conductivity of FinFET which appears to be gradually decreasing as the oxide thickness of the device increases along with drain current. Table 1 shows that the conductivity of FinFET appears to be maximum when the oxide thickness was 2nm which is  $2.66 \times 10^{-4}$  mho. Conductivity appears to be gradually decreasing and it reaches to  $1.48 \times 10^{-4}$  mho when the oxide thickness is 19nm which appears to be lower. (Table 2) shows that the conductivity of single gate MOSFET appears to be maximum when the oxide thickness was 2nm which is  $1.64 \times 10^{-4}$  mho.



**Fig. 1.** Simulated IV characteristics of FinFET for an oxide thickness of two gates (a) 2 nm (b) 5nm (c) 6 nm (d) 7 nm (e) 8 nm (f) 9 nm (g) 10 nm (h) 11 nm (i) 12 nm (j) 13 nm (k) 14 nm (l) 15 nm (m) 16 nm (n) 17 nm (o) 18 nm (p) 19 nm. The red line represents the IV curve with a drain voltage of 1v and the blue line represents IV curve with a drain voltage of 0.05v.

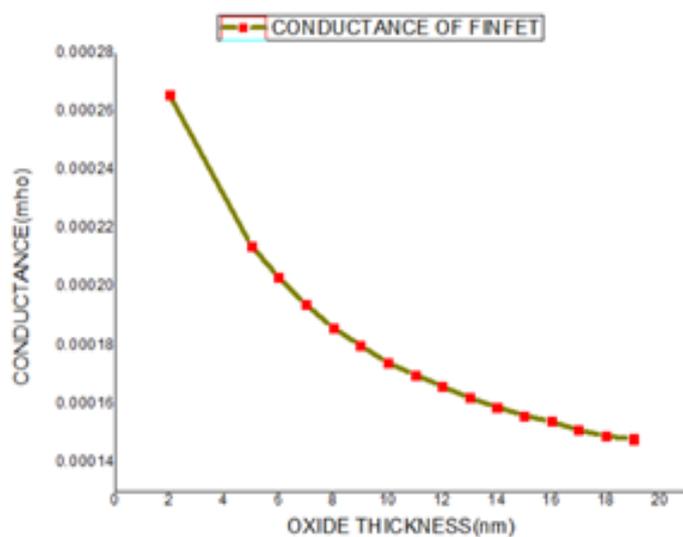
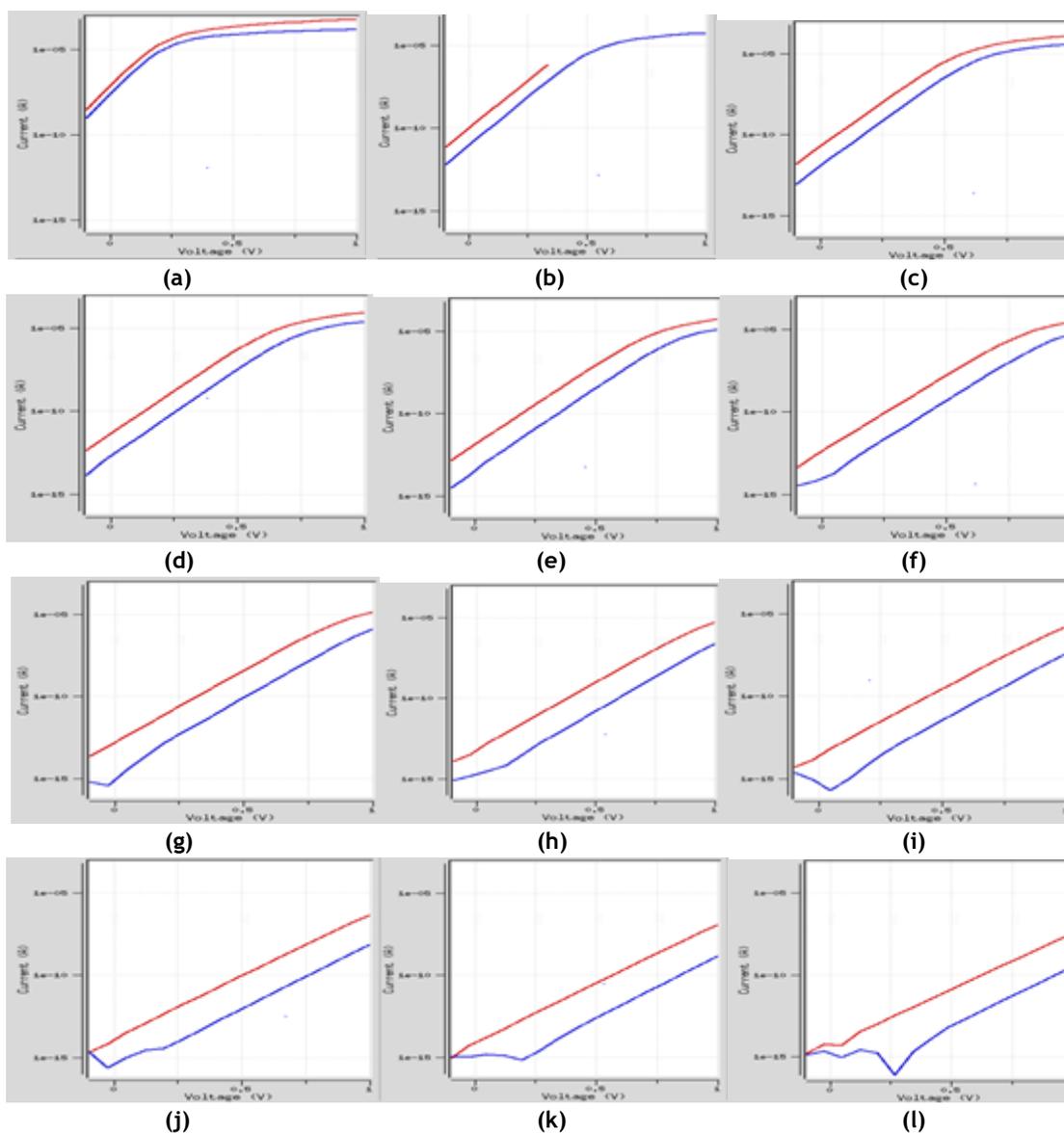
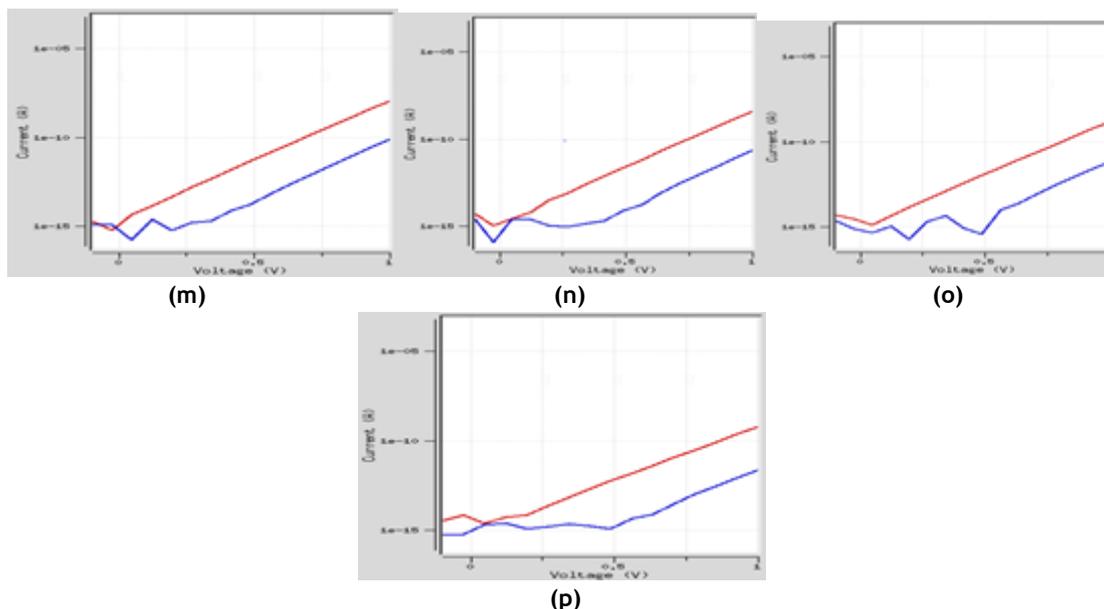


Fig. 2. Graphical representation of the conductivity of FinFET. Conductance of FINFIT appears to be inversely proportional to the thickness of the oxide layer.





**Fig. 3.** Simulated IV characteristics of Single gate MOSFET for oxide thickness of (a) 2 nm (b) 5 nm (c) 6 nm (d) 7 nm (e) 8 nm (f) 9 nm (g) 10 nm (h) 11 nm (i) 12 nm (j) 13 nm (k) 14 nm (l) 15 nm (m) 16 nm (n) 17 nm (o) 18 nm (p) 19 nm. The red line represents the IV curve with a drain voltage of 1V and the blue line represents IV curve with a drain voltage of 0.05 V.

**Table 1.** Drain current and conductance values for FINFET.

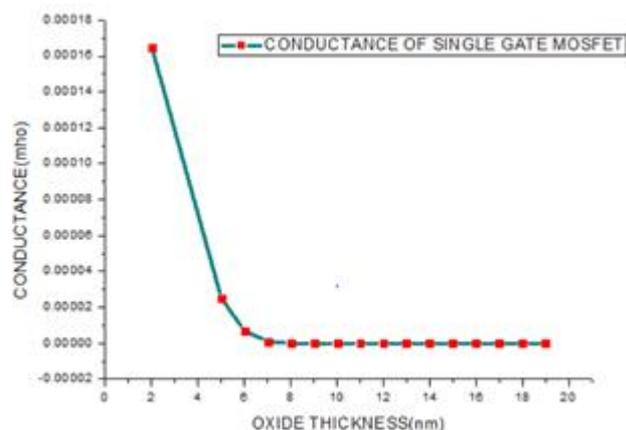
Oxide thickness (nanometer)	Current (amp)*10 <sup>4</sup>	Conductance (mho)*10 <sup>4</sup>
2	1.60	2.66
5	1.29	2.14
6	1.22	2.03
7	1.17	1.94
8	1.12	1.869
9	1.08	1.80
10	1.05	1.75
11	1.02	1.70
12	0.99	1.66
13	0.97	1.62
14	0.96	1.59
15	0.94	1.56
16	0.92	1.54
17	0.91	1.51
18	0.89	1.49
19	0.88	1.48

**Table 2.** Drain current and conductance values for single gate MOSFET

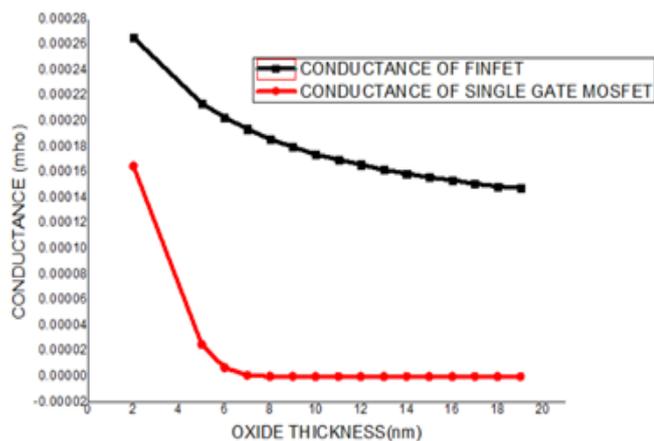
Oxide thickness (nanometer)	Current(amp)	Conductance(mho)
2	1.04e-04	1.64e-4
5	1.59e-05	2.51e-5
6	4.41e-06	6.96e-6
7	6.47e-07	1.02e-6
8	7.34e-08	1.15e-7
9	9.02e-09	1.42e-8
10	1.30e-09	2.06e-9
11	2.23e-10	3.52e-10
12	4.44e-11	7.02e-11
13	1.01e-11	1.60e-11
14	2.62e-12	4.15e-12
15	7.54e-13	1.19e-12
16	2.50e-13	3.95e-13
17	7.53e-14	1.19e-13
18	2.48e-14	3.92e-14
19	7.94e-15	1.25e-14

Conductivity appears to be gradually decreasing and it reaches to  $1.25 \times 10^{-14}$  mho when the oxide thickness is 19nm

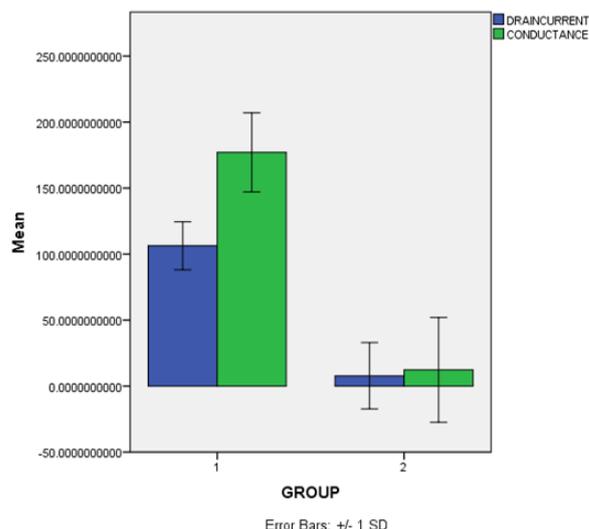
which appears to be the lowest among all the simulated values. (Fig 4) shows the graphical representation of the conductivity of single gate MOSFET which appears to be gradually decreasing as the oxide thickness of the device increases along with drain current. From the results obtained it appears that the conductance of FinFET is much higher than single gate MOSFET which is shown in (Fig 5). According to (Table-3) there is a statistically significant difference between the conductance and drain current of single gate MOSFET and FinFET since the value of p is less than 0.05 ( $p < 0.05$ ). (Table 4) shows that Conductance of FinFET has the highest mean 177.0625 and conductance of single gate MOSFET has the lowest mean 12.32. The drain current of FinFET has a mean of 106.3125 which is the higher value and single gate MOSFET has the lowest mean of 7.815.(Fig 6) shows the comparison of the mean of (+1 SD) conductance and drain current of FinFET and single gate MOSFET by varying oxide thickness.



**Fig. 4.** Graphical representation of the conductivity of single gate MOSFET. Conductance and oxide thickness are found to be inversely proportional to each other.



**Fig. 5.** Comparison of conductance of FinFET and MOSFET. Conductance of FinFET is found to be significantly better than single gate MOSFET.



**Fig. 6.** Bar chart comparing the mean of (+1 SD) conductance and drain current of FinFET and single gate MOSFET by varying oxide thickness. There is a significant difference between the two groups  $p < 0.05$  (Independent Sample T Test). X-AXIS: FinFET and single gate MOSFET. Y-AXIS: Mean conductance and Mean drain current.

**Table 3.** T-test Comparison of conductance of FinFET and single gate MOSFET by varying the oxide thickness ranging from 2nm to 20nm. There is a Statistically significant difference in conductance of FinFET and single gate MOSFET. Conductance of FinFET has the highest mean (177.063) over single gate MOSFET(12.32). Drain current of FinFET has a mean of 106.3125 which is higher and single gate MOSFET has the lowest mean of 7.815.

GROUP		N	Mean	Std. Deviation	Std. Error Mean
DRAIN CURRENT	FinFET	320	106.313	18.2037	1.0176
	SG-FET	320	7.81504	25.1783	1.4075
CONDUCTANCE	FinFET	320	177.06	29.983	1.676
	SG-FET	320	12.325	39.704	2.219

**Table 4.** The Mean, standard deviation and significance difference of conductivity and drain current for single gate MOSFET and FinFET. There is a significance difference between the two groups since  $p < 0.05$  (Independent Sample T Test)

		Levene's test for Equality of variances		t-test for equality of means						
		f	sig	t	df	Sig. (2-tailed)	Mean difference	Std. Error Difference	95% confidence Interval of the Difference	
Drain current	Equal variances assumed	0.283	0.595	56.710	638	0.000	98.49745430	1.736847160	95.08682625	101.9080823
	Equal variance not assumed			56.710	580.926	0.000	98.49745430	1.736847160	95.08682625	101.9087193
Conductance	Equal variances assumed	0.849	0.357	59.229	638	0.000	164.7367685	2.781335591	159.2750898	170.1984472
	Equal variance not assumed			59.229	593.544	0.000	164.7367685	2.781335591	159.2750898	170.1992248

### Discussion

Current and voltage characteristics of FinFET and single gate MOSFET are analysed by varying the oxide thickness of the device. The drain current vs gate voltage characteristics have been simulated for a different oxide thickness of the device ranging from 2nm to 20nm. After analysing the simulation curves, it has been observed that lowering the oxide thickness of the device will result in the increase of the drain current which ultimately increases the conductivity for both single gate MOSFET and FinFET.

The factors that affect the conductance of FinFET and single gate MOSFET in this research work are oxide thickness, source/drain length, channel dimension, substrate thickness and junction depth. The other factors are kept constant and simulations are carried out by varying oxide thickness. As the

oxide thickness of FinFET and single gate MOSFET increases the conductivity and drain current decreases (Kuhn 2011), (Kato et al. 2014), (Reddick and Amaratunga 1995). The oxide thickness is modified between 2nm and 20nm for both FinFET and single gate MOSFET.

Ren analysed that, because of the application in CMOS IC circuit fabrication FINFET devices are carefully investigated. Reducing MOSFET size has an extraordinary effect on electrostatic characteristics. The unpredictable variations of the characteristics lead to a dissimilar impact which is basic according to the perspective of design and manufacture. The behaviour of hole mobility in multi-gate devices is obviously of great importance (Ren et al. 2002), (Huang et al., n.d.). Ren work is not similar to the current

research work since it deals with the optimization of conductance of the device.

Our institution is passionate about high quality evidence based research and has excelled in various fields (Vijayashree Priyadharsini 2019; Ezhilarasan, Apoorva, and Ashok Vardhan 2019; Ramesh et al. 2018; Mathew et al. 2020; Sridharan et al. 2019; Pc, Marimuthu, and Devadoss 2018; Ramadurai et al. 2019). We hope this study adds to this rich legacy.

Due to the limitations such as short channel effects, narrow channel effects, subthreshold conduction and channel length modulation the power passing through the devices is dissipated in the form of current leakage which decreases the conductance and performance of single gate MOSFET. Even though there is current leakage in FinFET, it is minimal when compared to current leakage of single gate MOSFET. Single gate MOSFET has only one gate so control over the channel is less which causes current leakage but FinFET has two fins along with two gates which provides better control over the channel and reduces the current leakage compared to single gate MOSFET. Due to these reasons FinFET is the replacement for single gate MOSFET since it provides better conductivity and performance when provided with the same input voltage.

In future, novel transistors like FinFET can be scaled down even further which can be used to fabricate high performance computing devices with less power consumption. (Park et al. 2006), (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003).

## Conclusion

FINFET gives better conductivity and performance compared to single gate MOSFET when provided with the same gate voltage. Current and voltage characteristics of FINFET and single gate MOSFET were explored through simulations by varying oxide thickness of the device ranging from 2nm to 20nm. The variation in current and voltage characteristics of FINFET and single gate MOSFET were analysed and results of FINFET were compared with single gate MOSFET by keeping gate voltage as constant (0.6v). After analysing the results it is clear that the conductance of both FINFET and single gate MOSFET decreases as oxide thickness increases. To improve the conductivity of FINFET and single gate MOSFET the oxide thickness should be minimum. Even though conductance increases by decreasing oxide thickness, FINFET is preferred over single gate MOSFET due to the presence of current leakage. Hence, FINFET can be the replacement for single gate MOSFET.

## Declarations

### Conflict of Interests

No conflict of interest in this manuscript.

### Author Contribution

Author T. Kiran Kumar Reddy was involved in data collection, data analysis, manuscript writing. Author Dr. A. Deepak was involved in conceptualization, guidance and critical review of manuscript.

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All the simulations used in this research paper were carried out in NanoHub and the data was processed in the tool and graphs were generated. The authors would like to express their gratitude towards Saveetha School of Engineering, Saveetha Institute of Medical and Technical Sciences (Formerly Known as Saveetha University) for providing the necessary infrastructure to carry out this work successfully.

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3. Saveetha Institute of Medical and Technical Sciences.
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